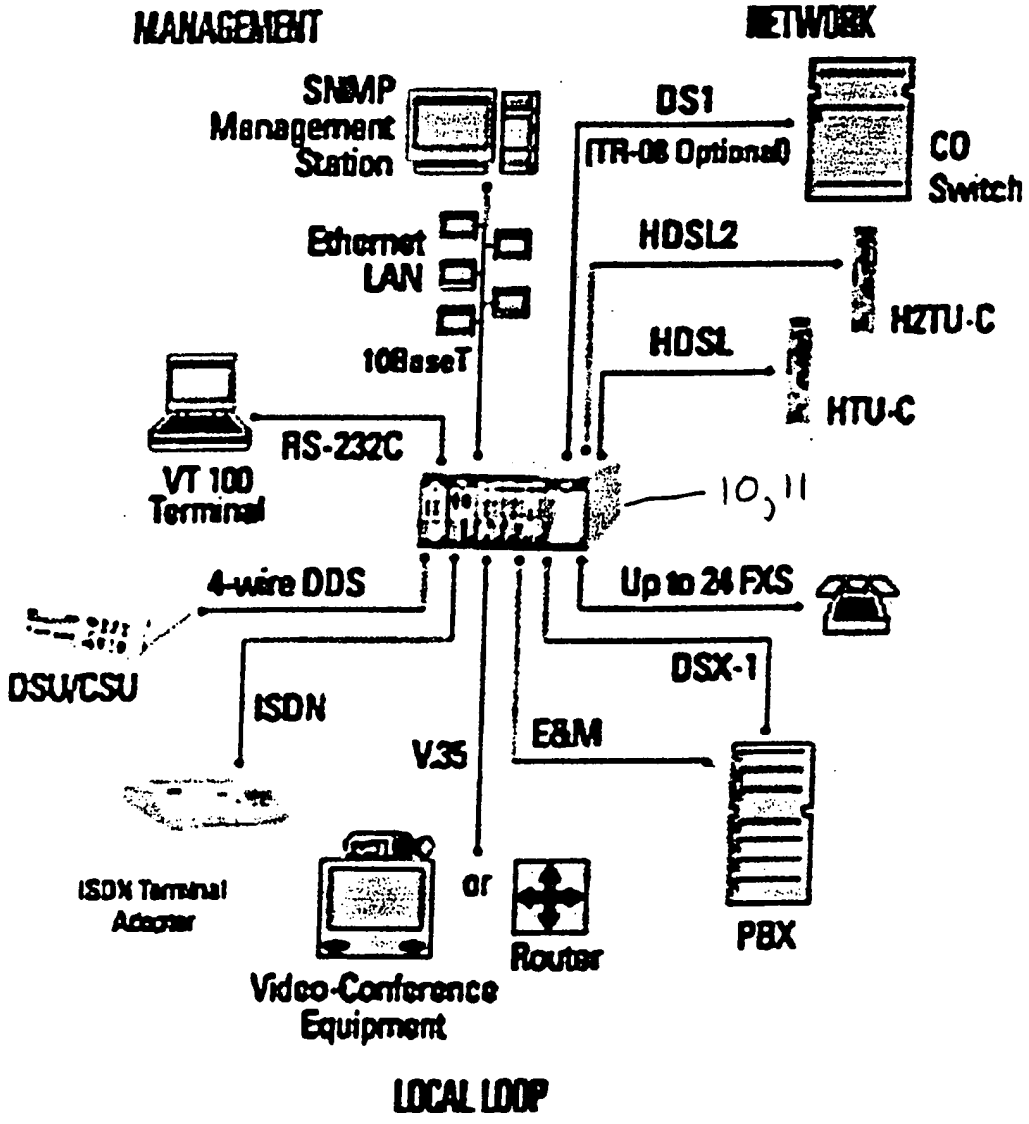

MANAGEMENT
NETWORK
SNMP
Management
Station
DS1
(TR-08 Optional)
CO
Switch
Ethernet
LAN
10BaseT
HDSL2
HZTU-C
HDSL
HTU-C
RS-232C
VT 100
Terminal
10, 11
4-wire DDS
Up to 24 FXS
DSU/CSU
DSX-1
ISDN
V.35
E&M
ISDN Terminal
Adapter
or
Router
PBX
Video-Conference
Equipment
LOCAL LOOP

FIG. 1

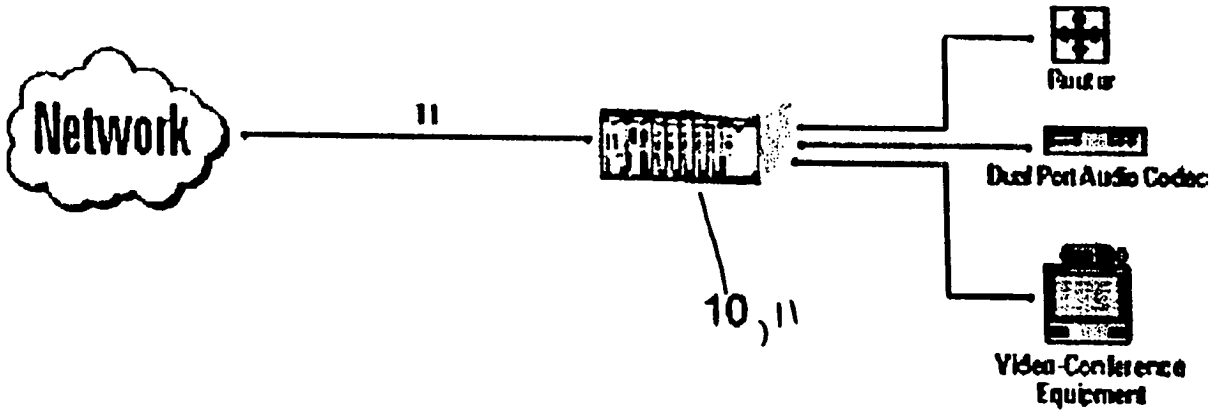

Network
11
Dual Port Audio Codec
10,11
Video-Conference
Equipment

FIG. 2

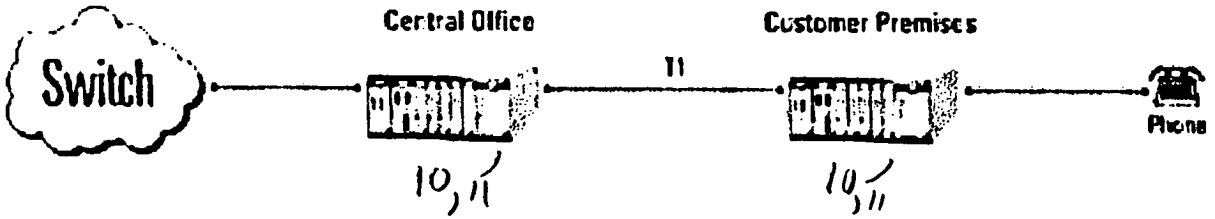

Switch
Central Office
T1
Customer Premises
Phone
10,11
10,11

FIG. 4(a)

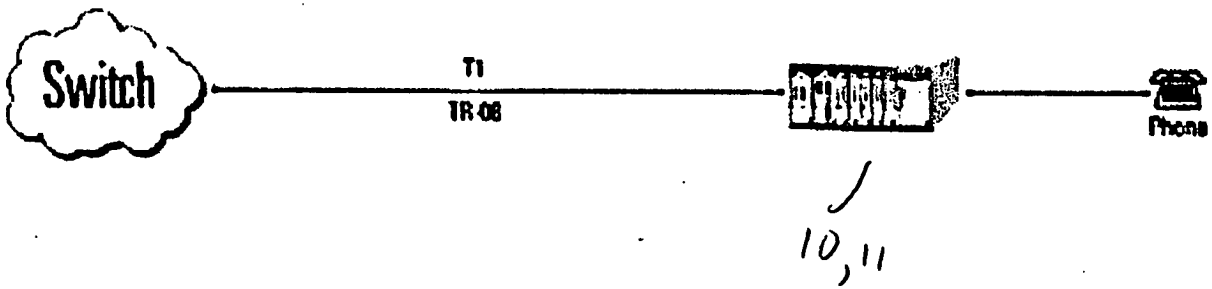

Switch
T1
TR 08
Phone
10,11

FIG. 4(b)

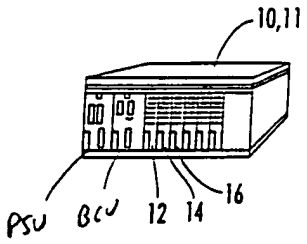


FIG. 5

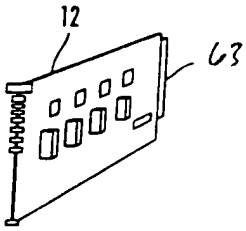


FIG. 6

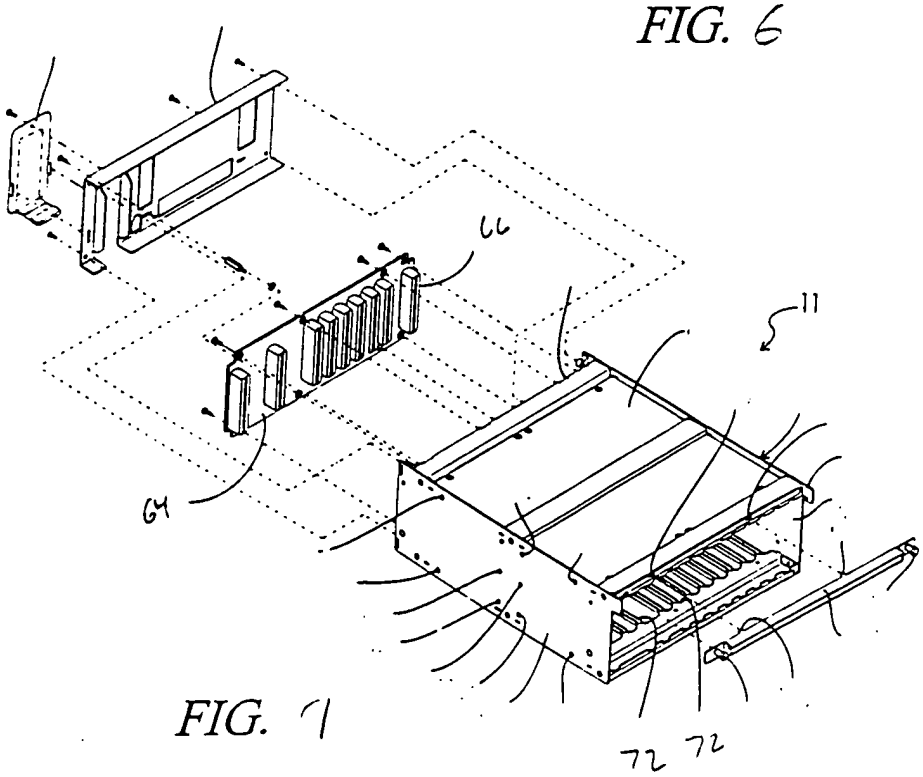


FIG. 7

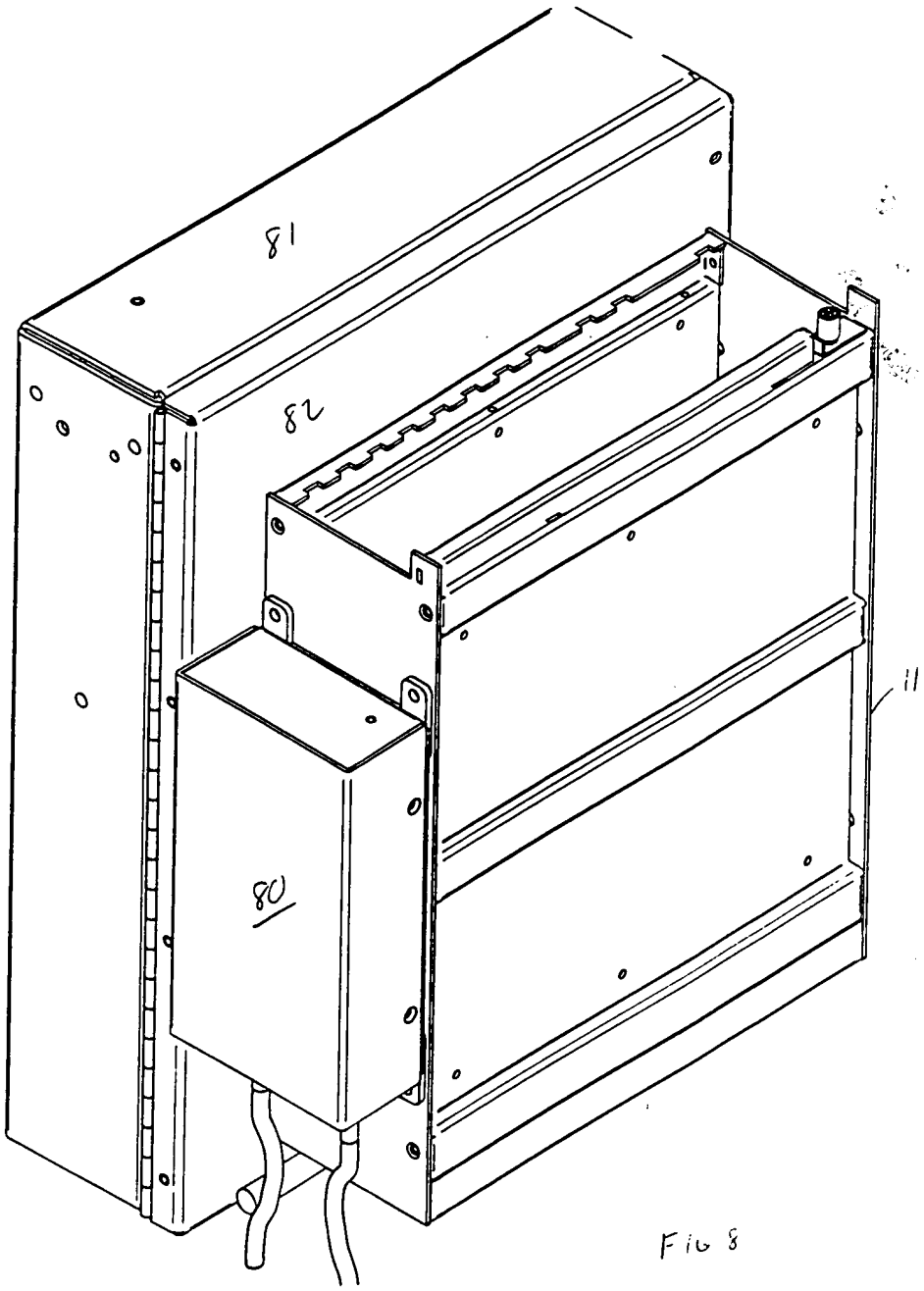


Fig 8

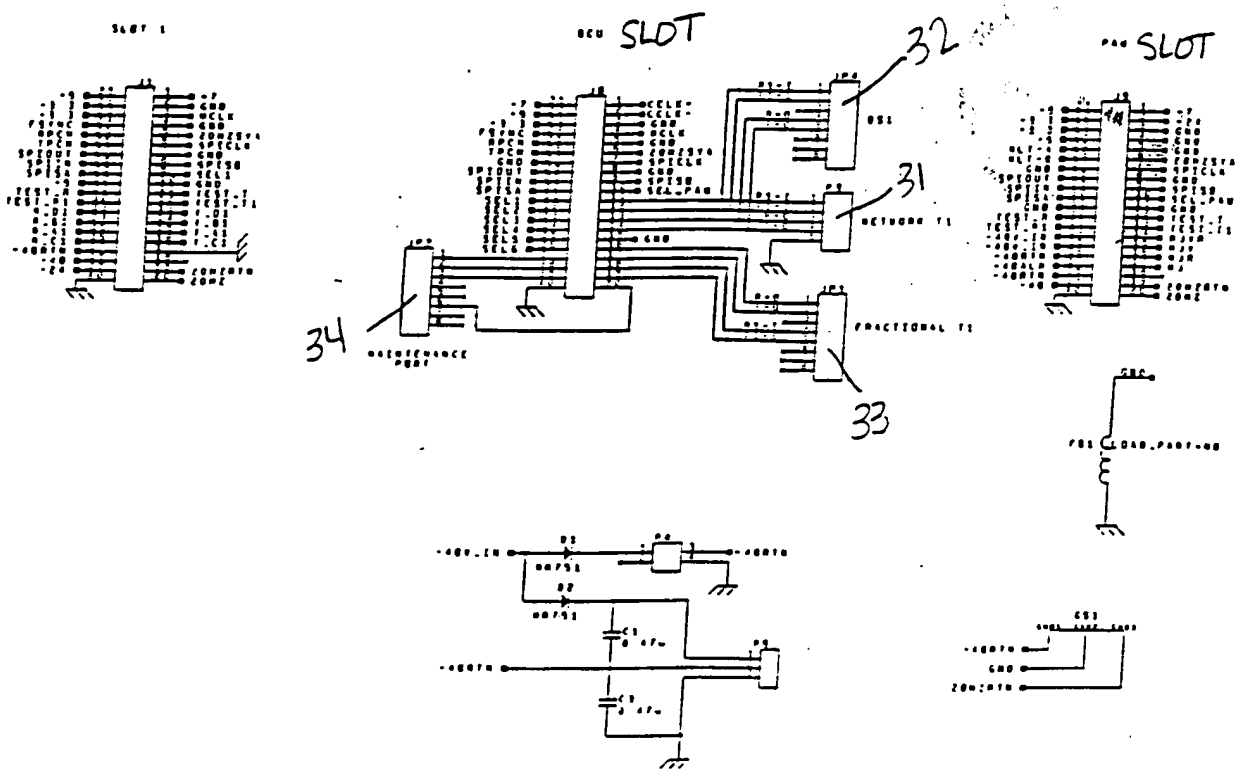
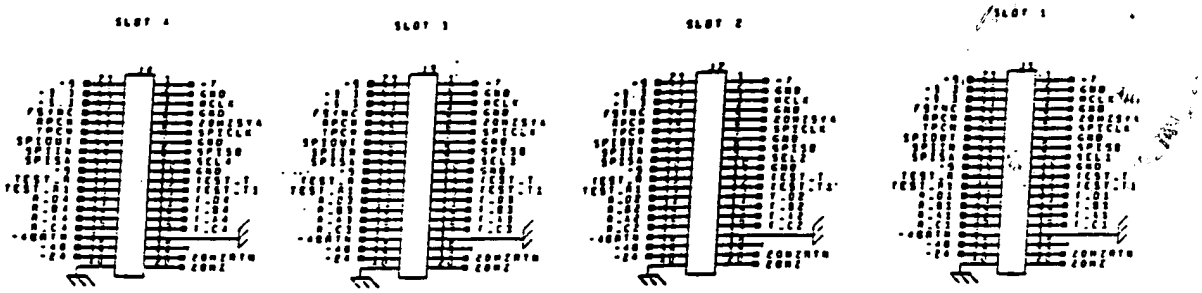
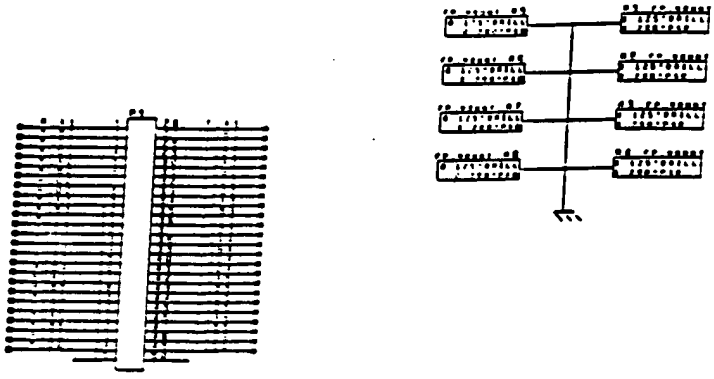
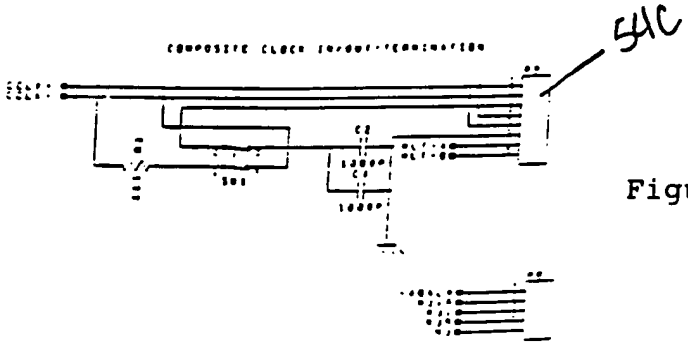


Figure 9



34





54C

Figure 9 (Continued)

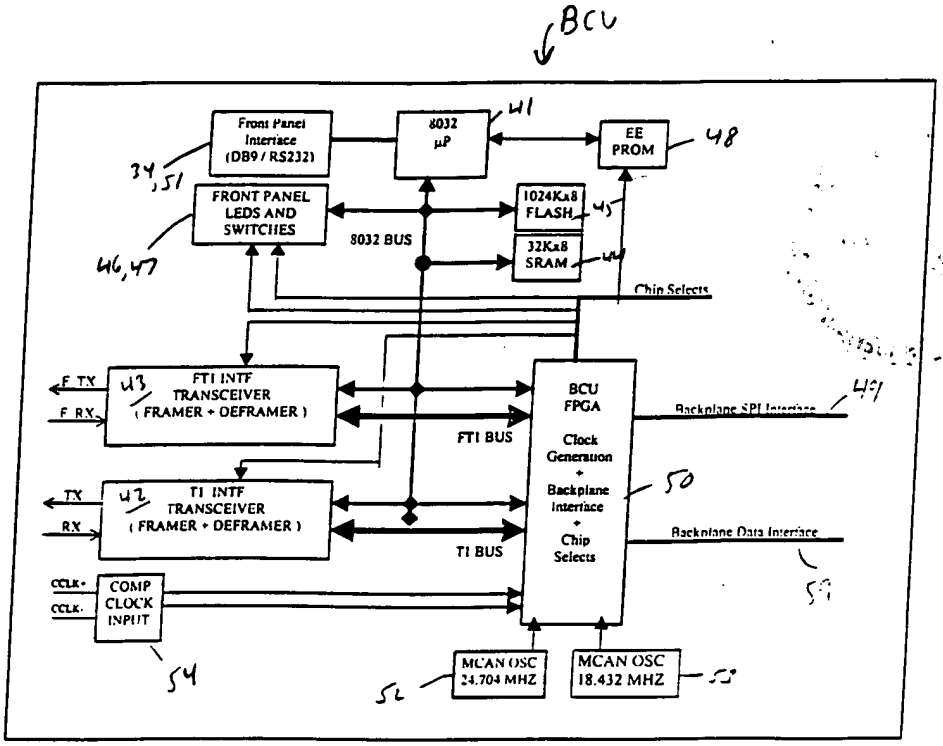

BCU
Front Panel Interface (DB9 / RS232)
8032 µP
EE PROM
FRONT PANEL LEDS AND SWITCHES
8032 BUS
1024Kx8 FLASH
32Kx8 SRAM
Chip Selects
F_TX
F_RX
FTI INTF TRANSCEIVER (FRAMER + DEFRAMER)
FTI BUS
BCU FPGA
Clock Generation
Backplane Interface
Chip Selects
Backplane SPI Interface
Backplane Data Interface
TX
RX
T1 INTF TRANSCEIVER (FRAMER + DEFRAMER)
T1 BUS
CCLK+
CCLK-
COMP CLOCK INPUT
MCAN OSC 24.704 MHZ
MCAN OSC 18.432 MHZ

Fig. 10

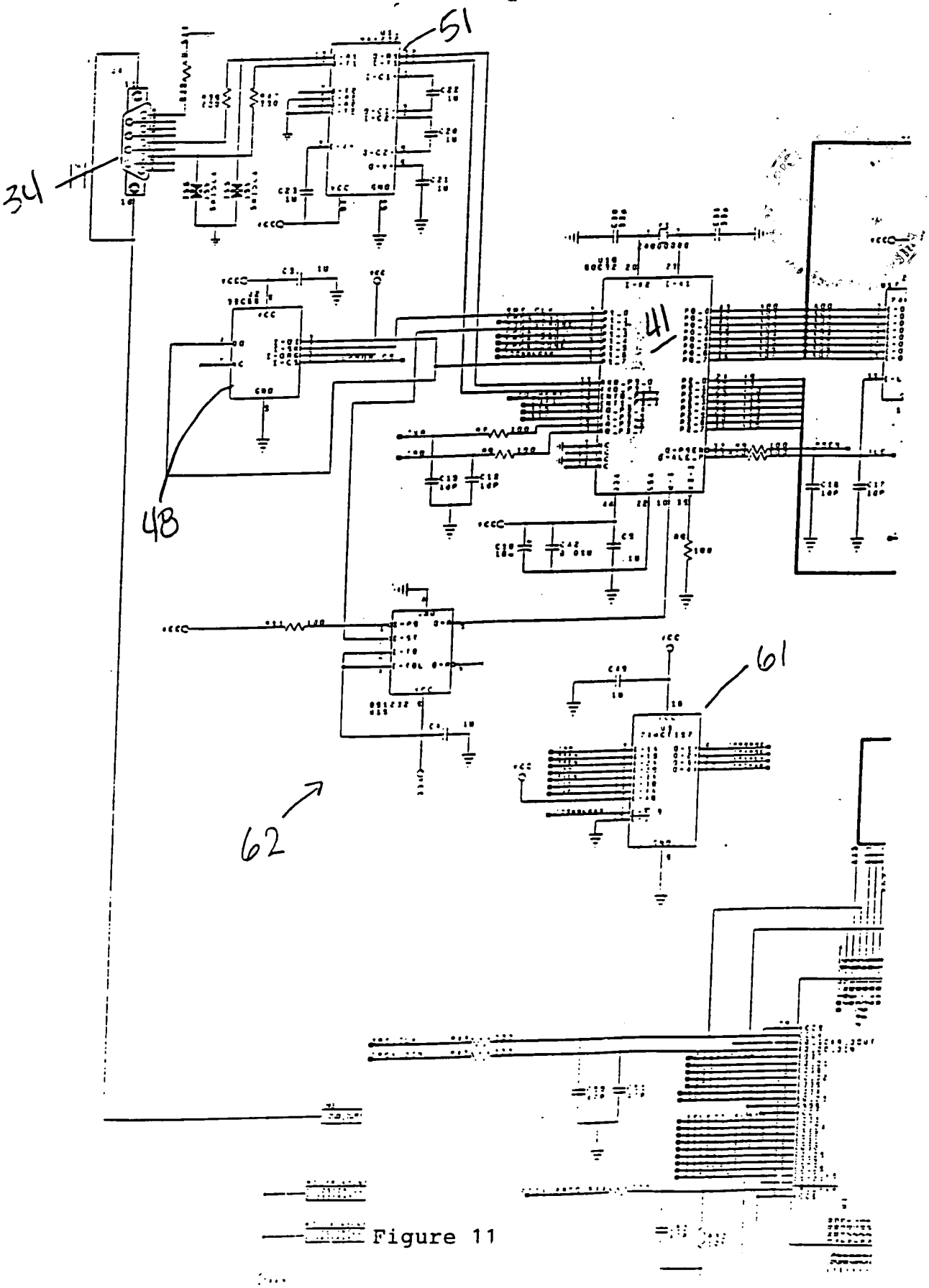
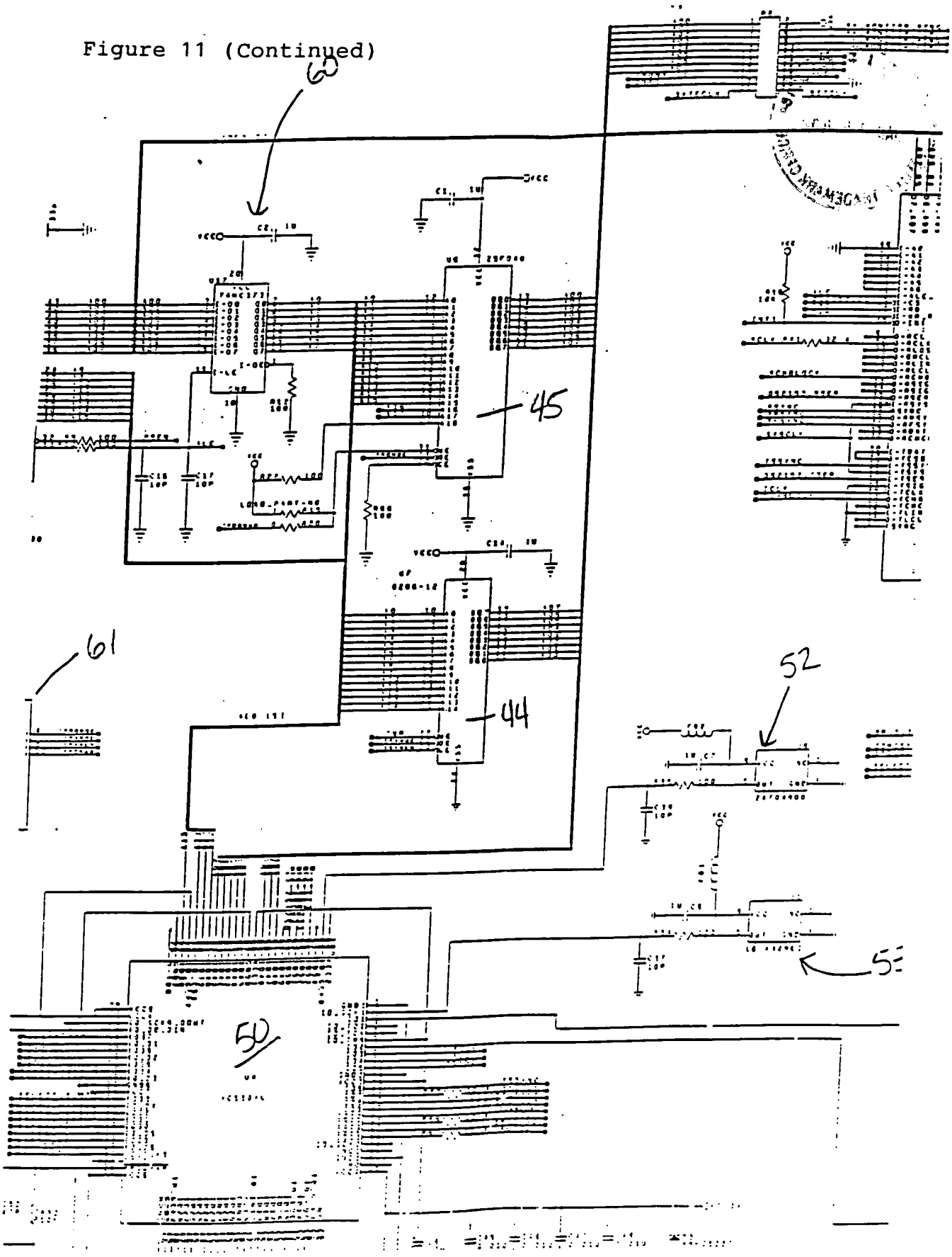


Figure 11

Figure 11 (Continued)



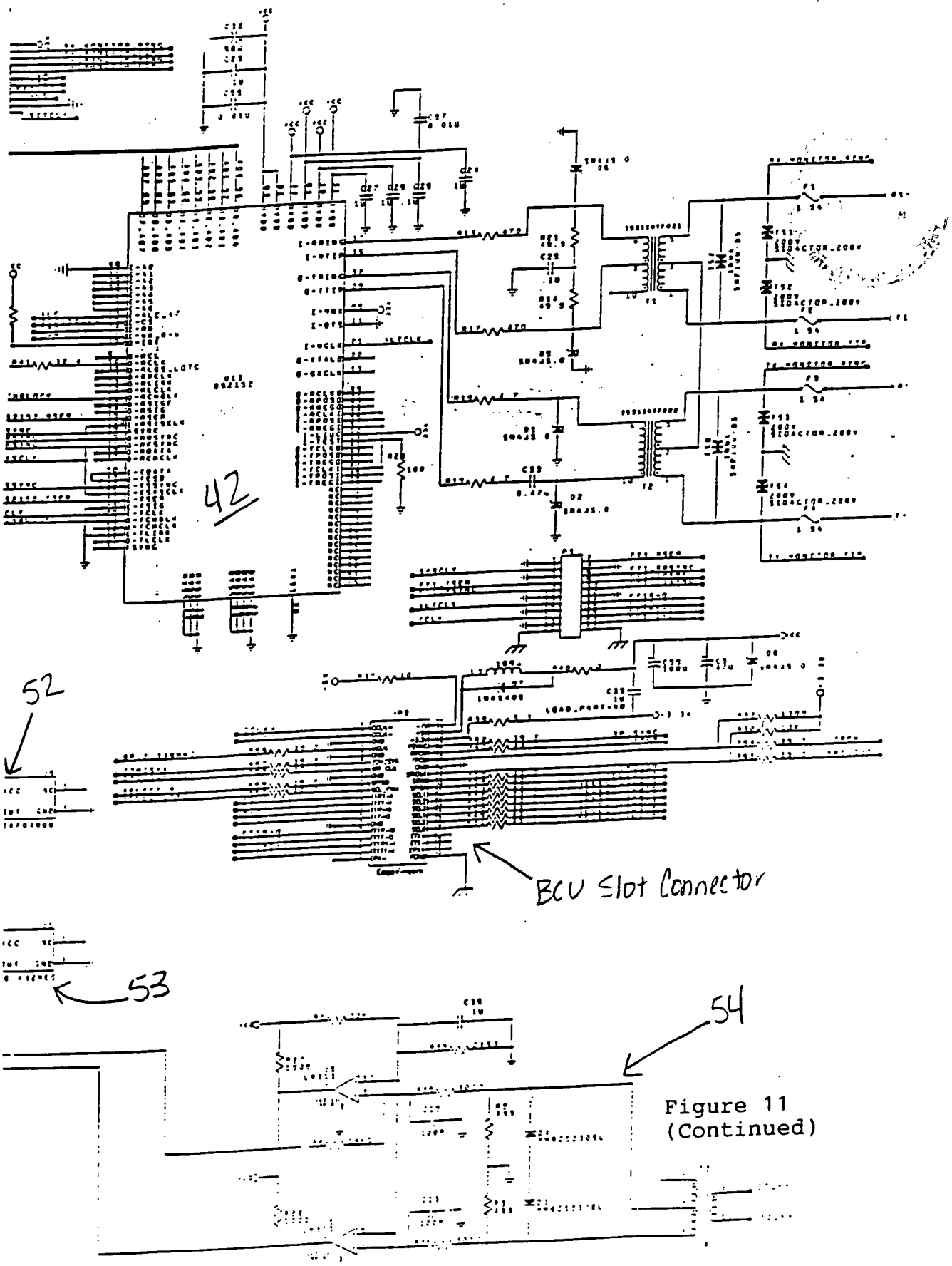


Figure 11
(Continued)

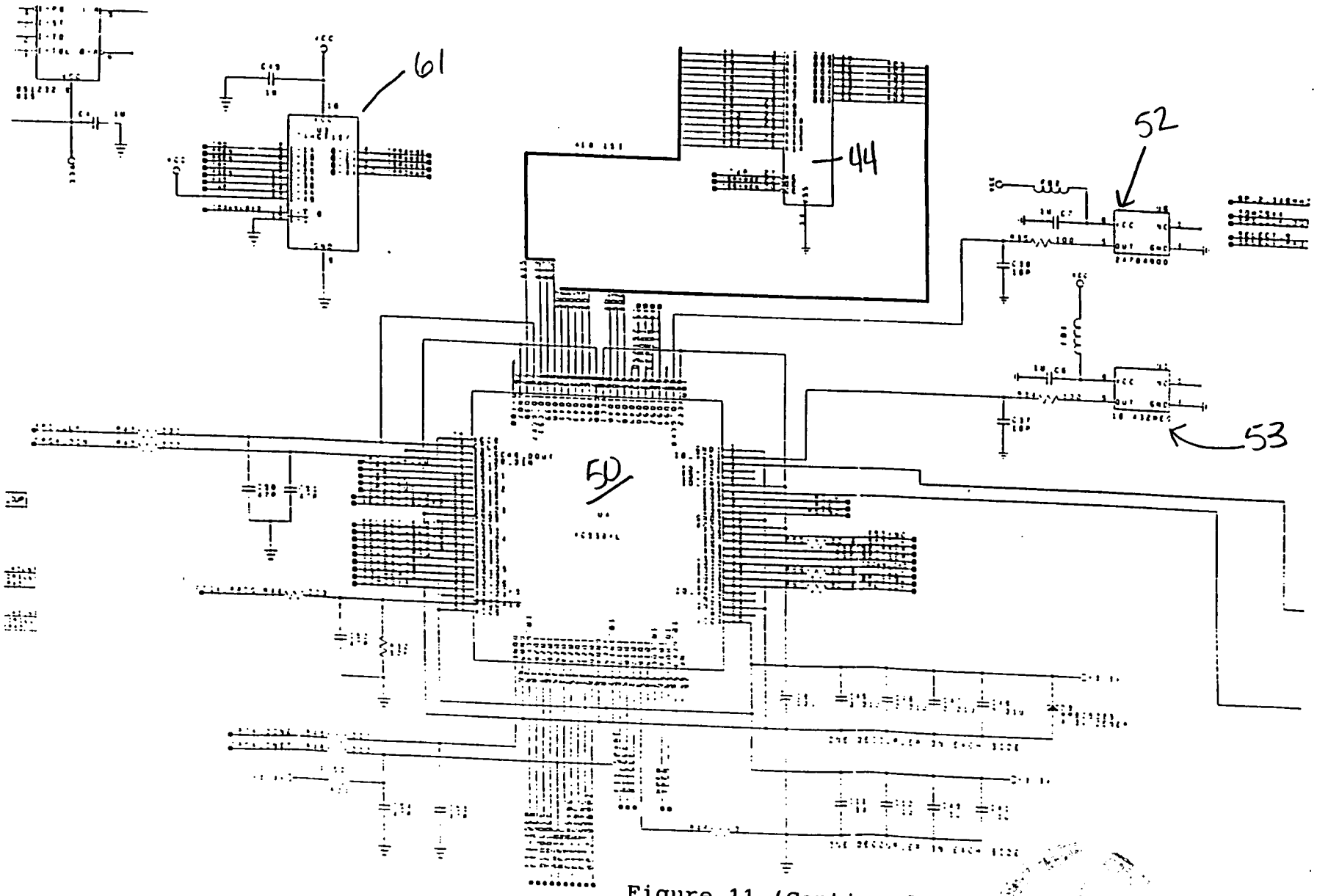


Figure 11 (Continued)

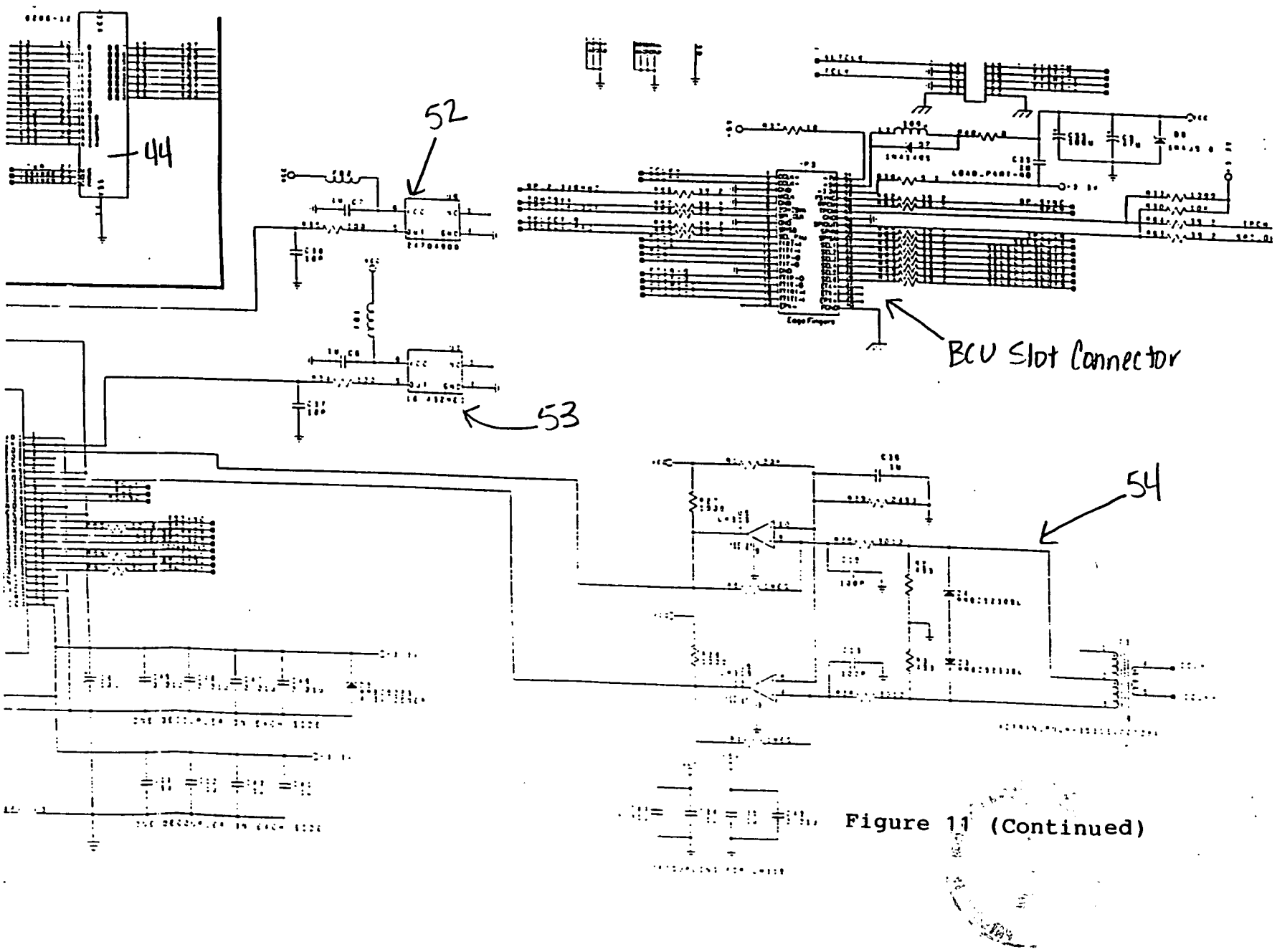


Figure 11 (Continued)

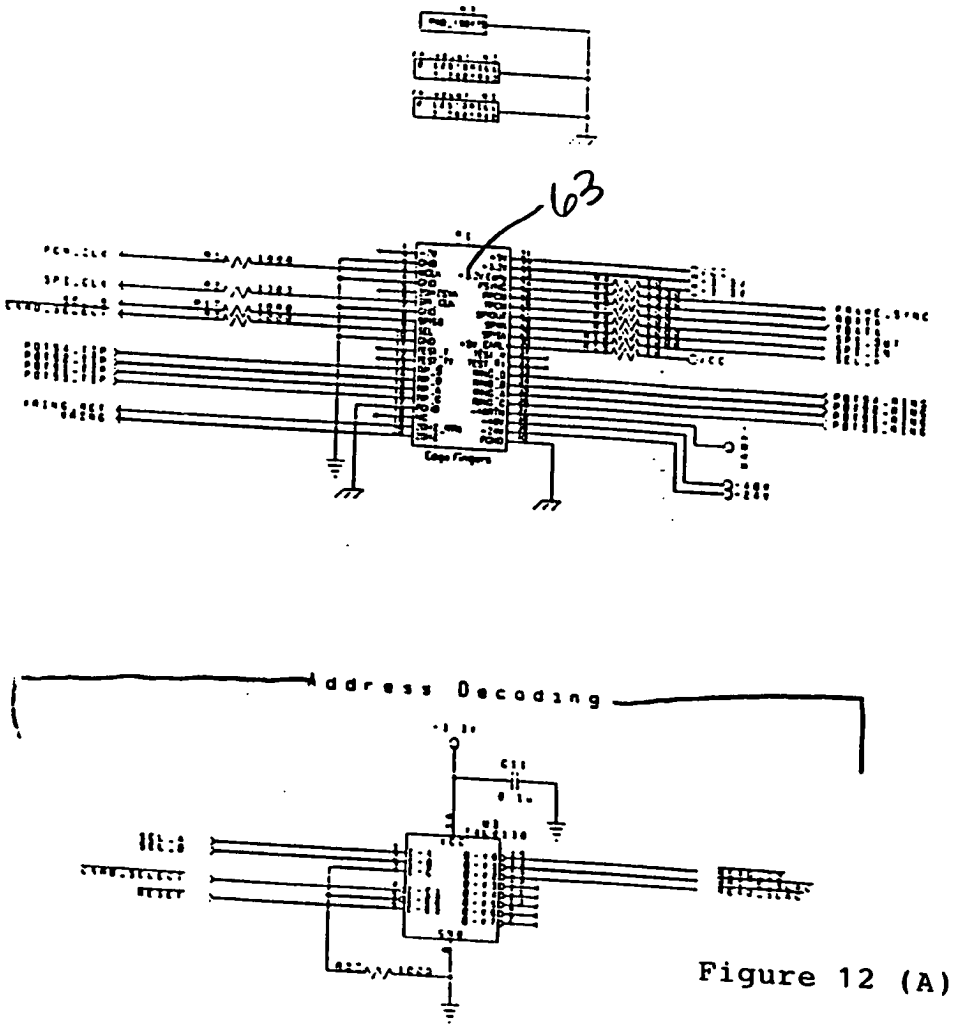
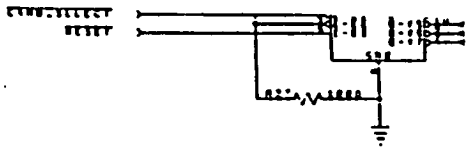
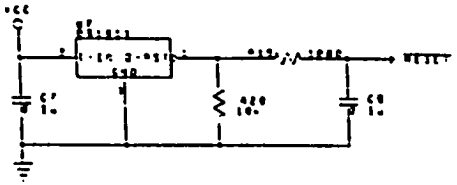


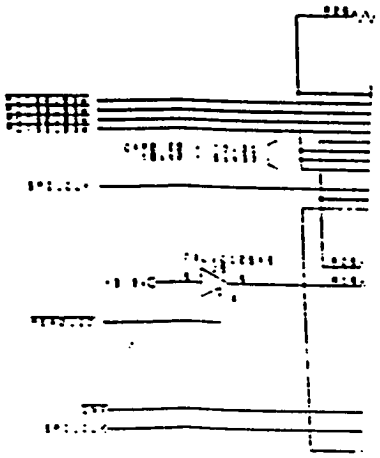
Figure 12 (A)



Power Monitor



Interrupt Card



Decoupling Capacitors

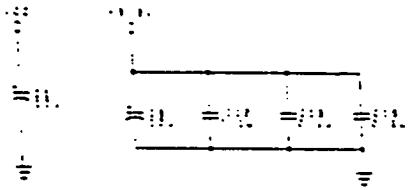


Figure 12(A) (Continued)

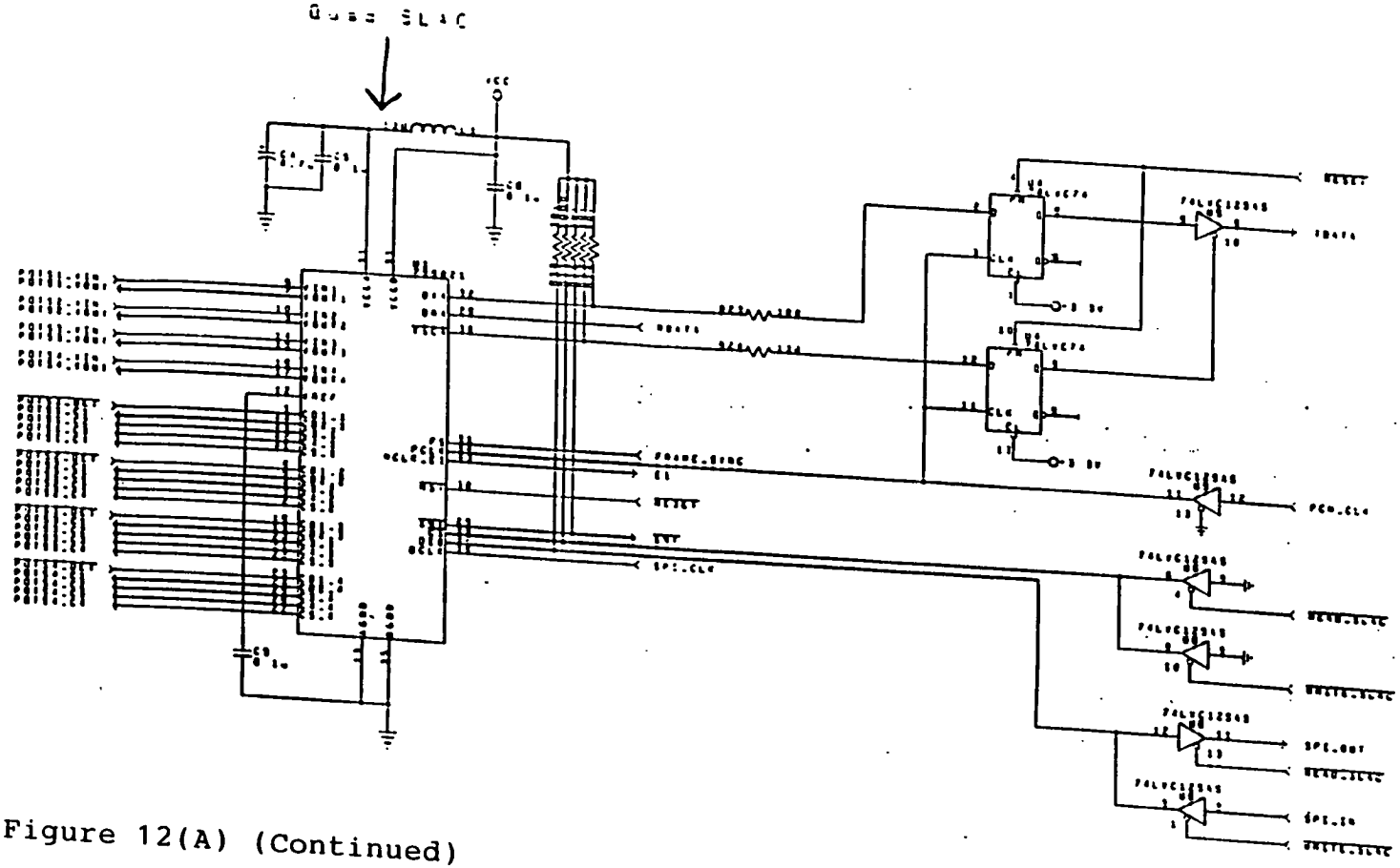


Figure 12(A) (Continued)

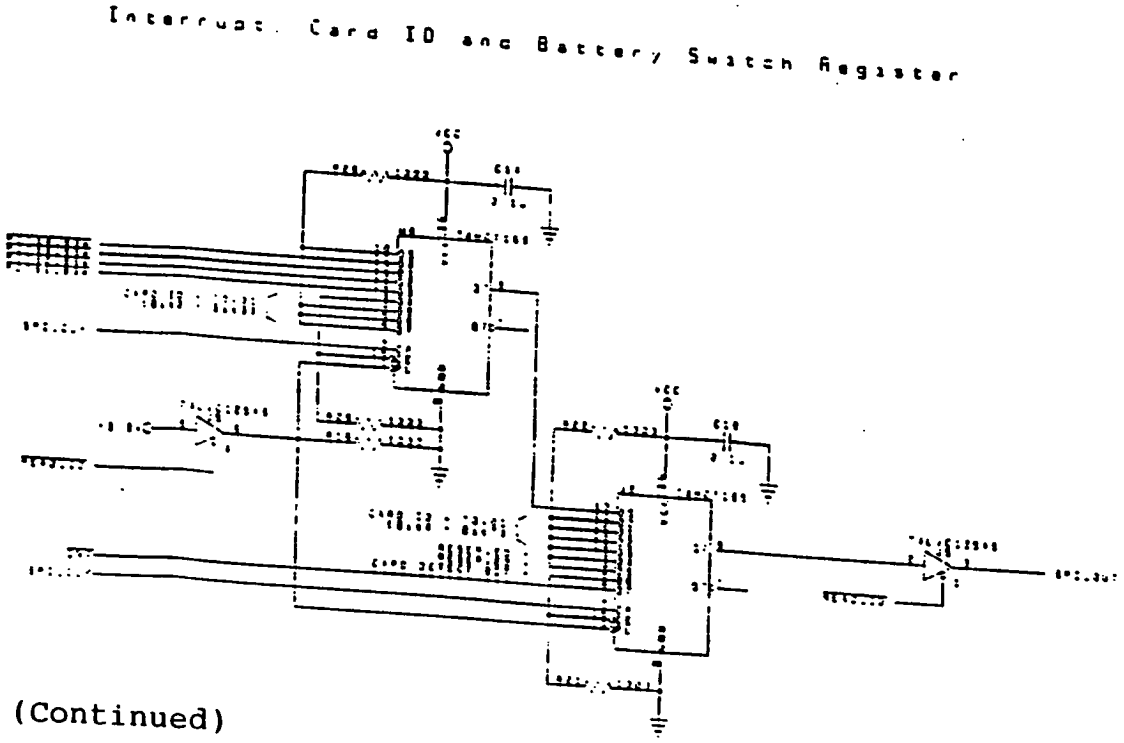


Figure 12(A) (Continued)

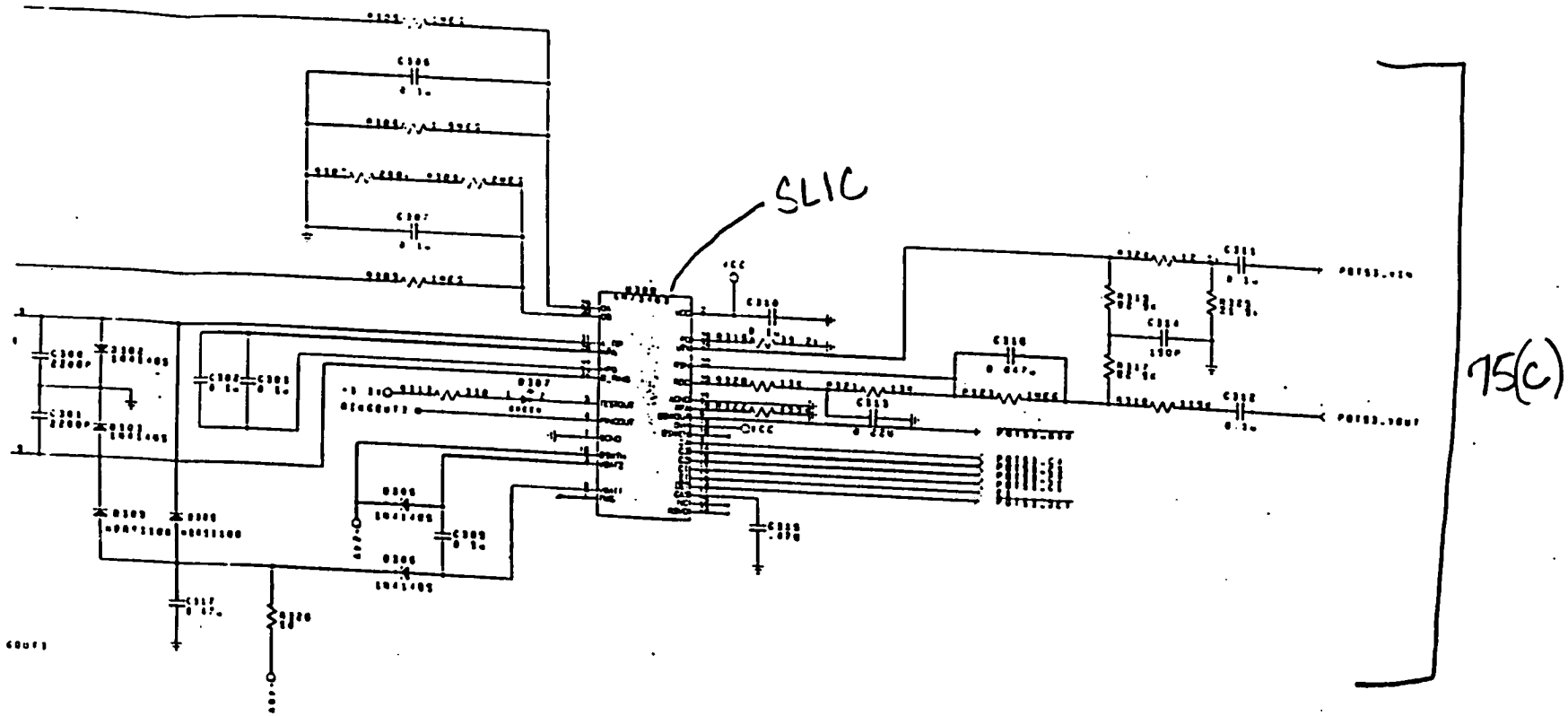


Figure 12(B)

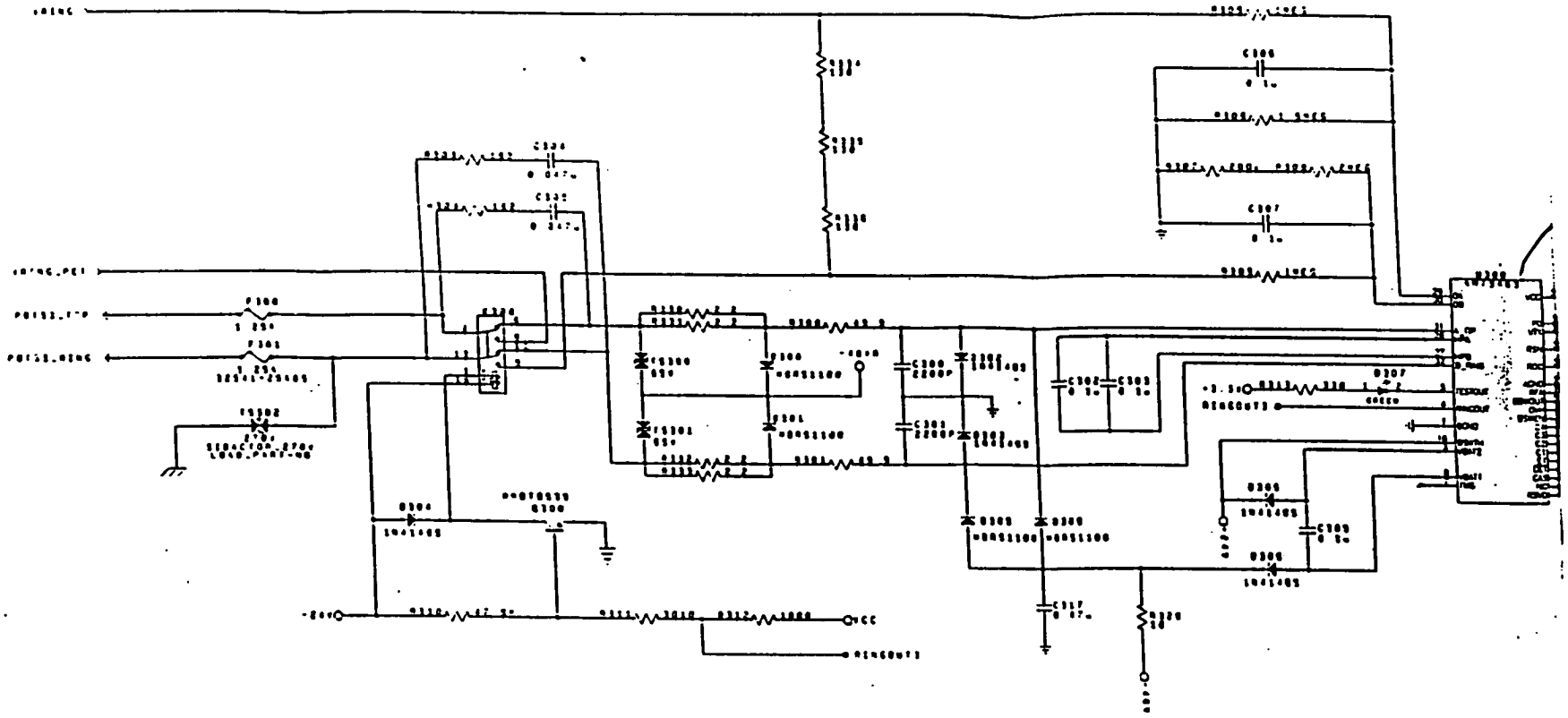


Figure 12(B) (Continued)

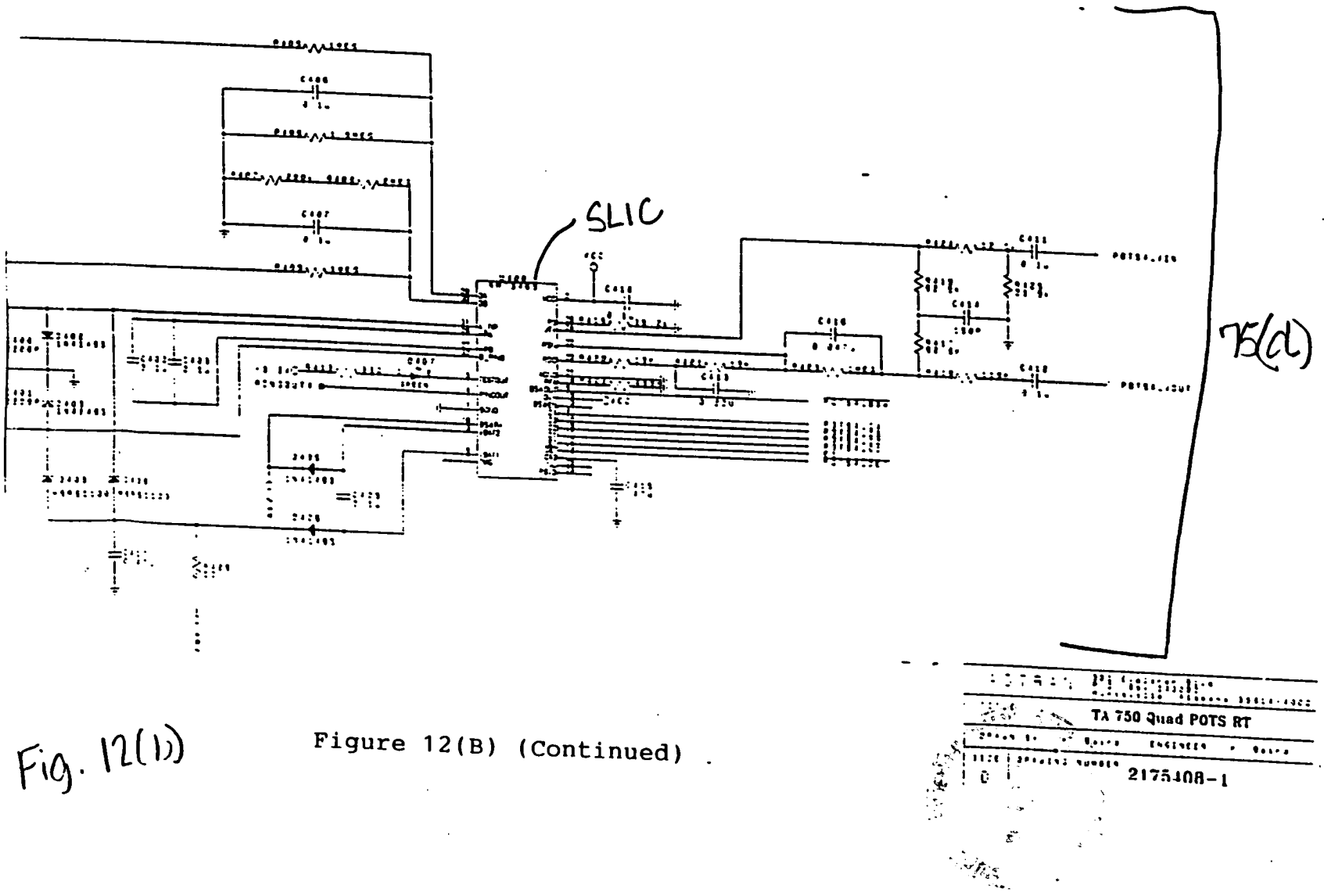


Fig. 12(1))

Figure 12(B) (Continued)

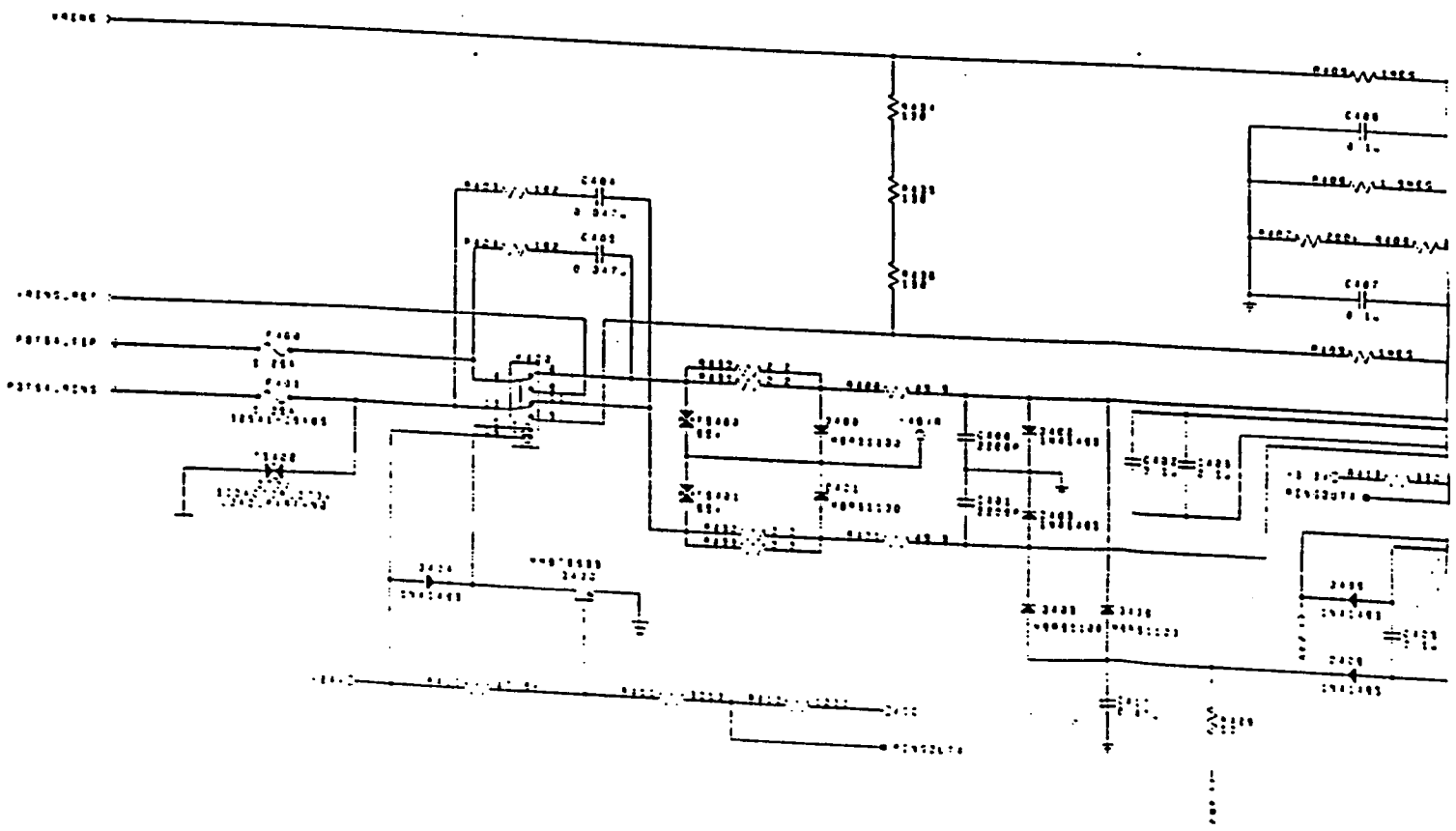


Figure 12(B) (Continued)

Fig. 12(B)

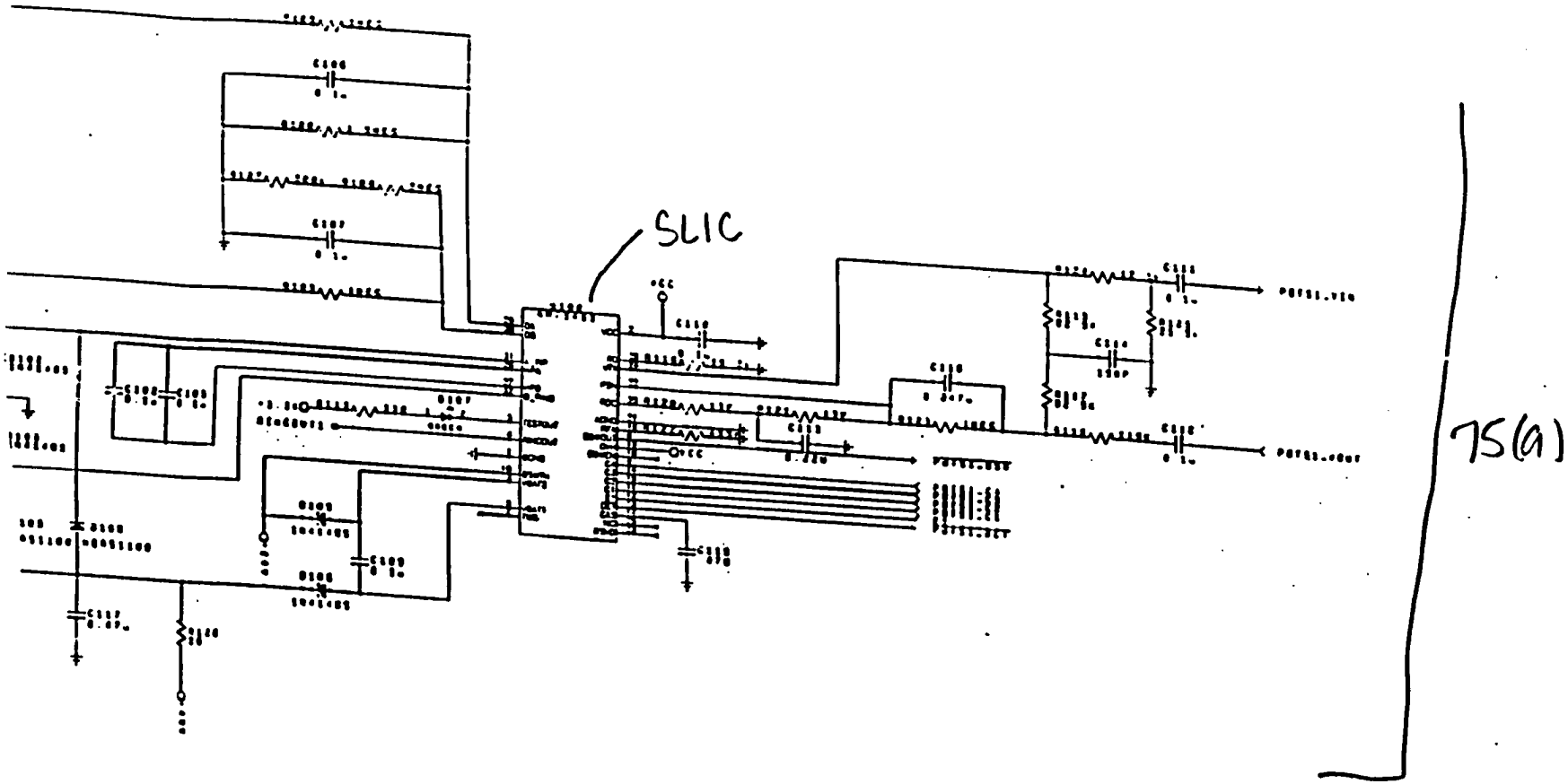


Figure 12(C)

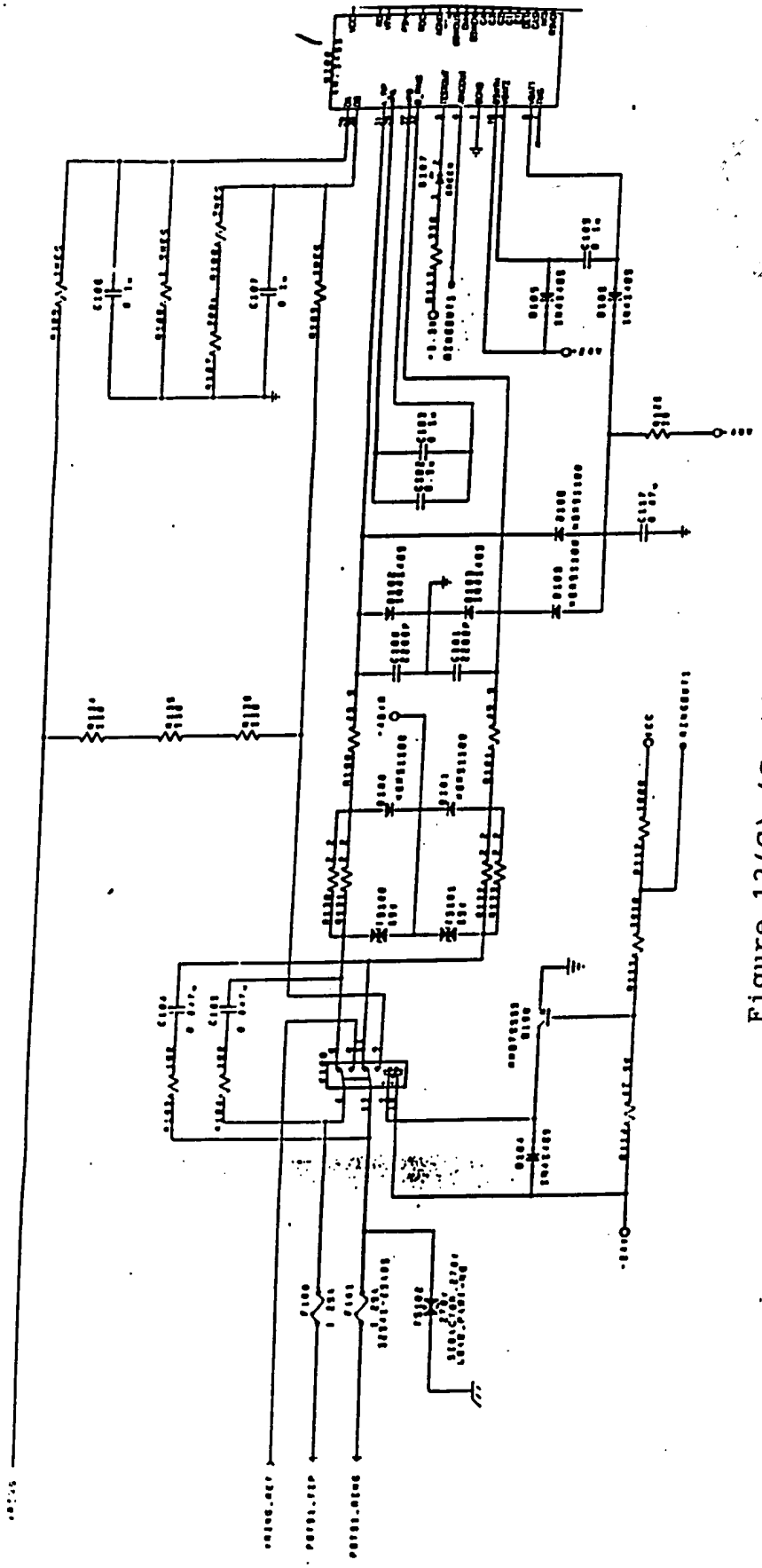


Figure 12(C) (Continued)

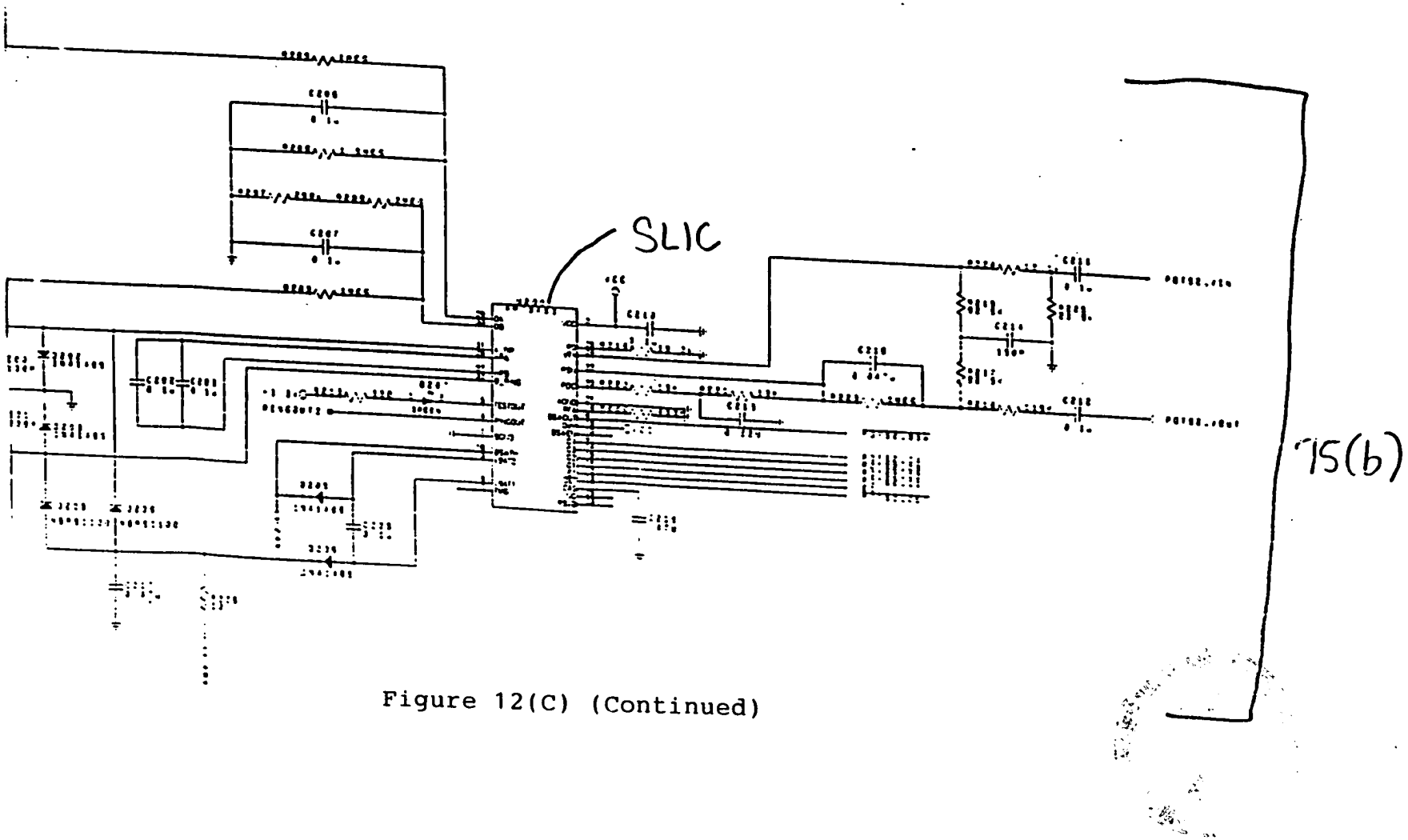


Figure 12(C) (Continued)

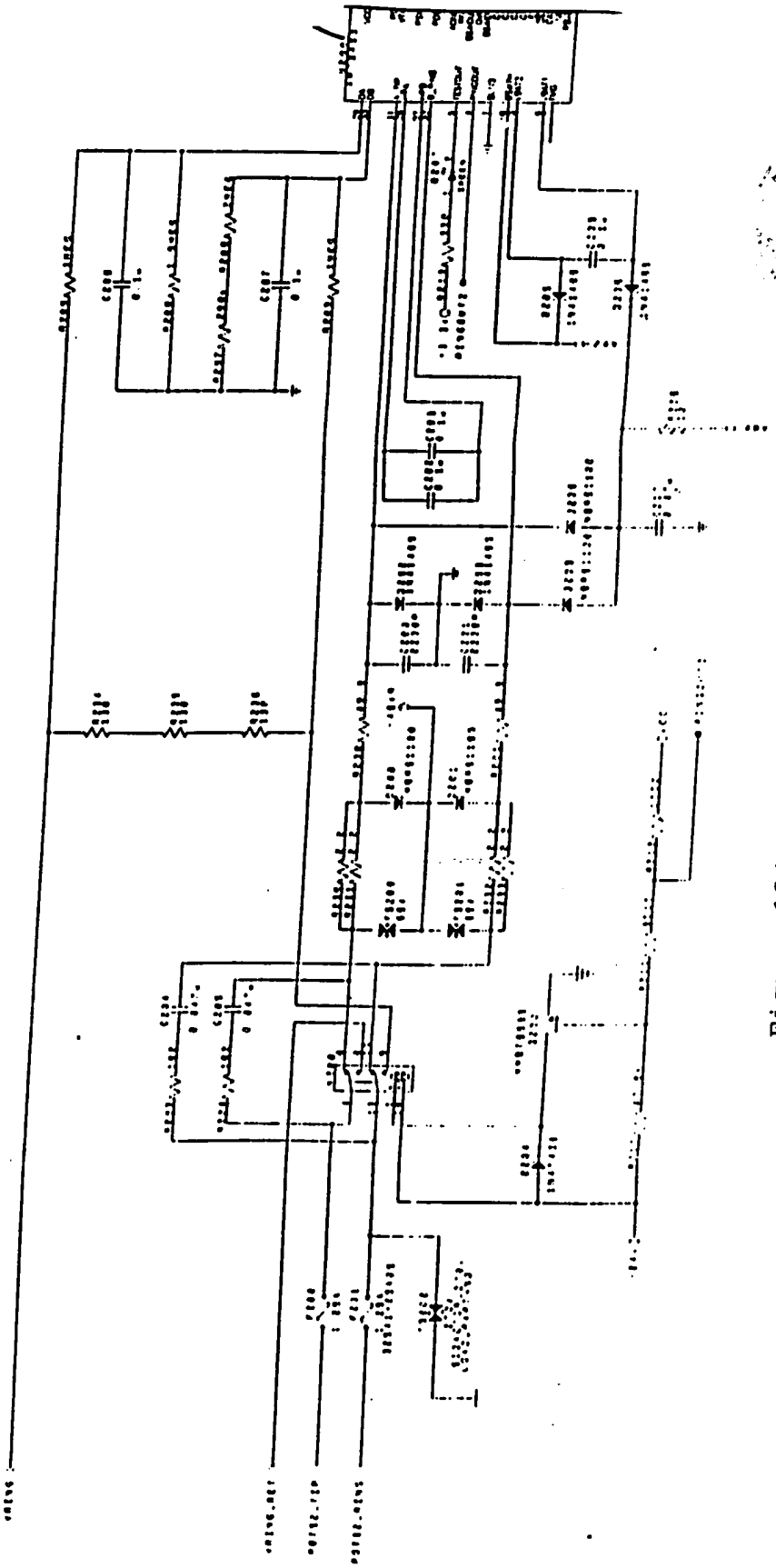


Figure 12(C) (Continued)

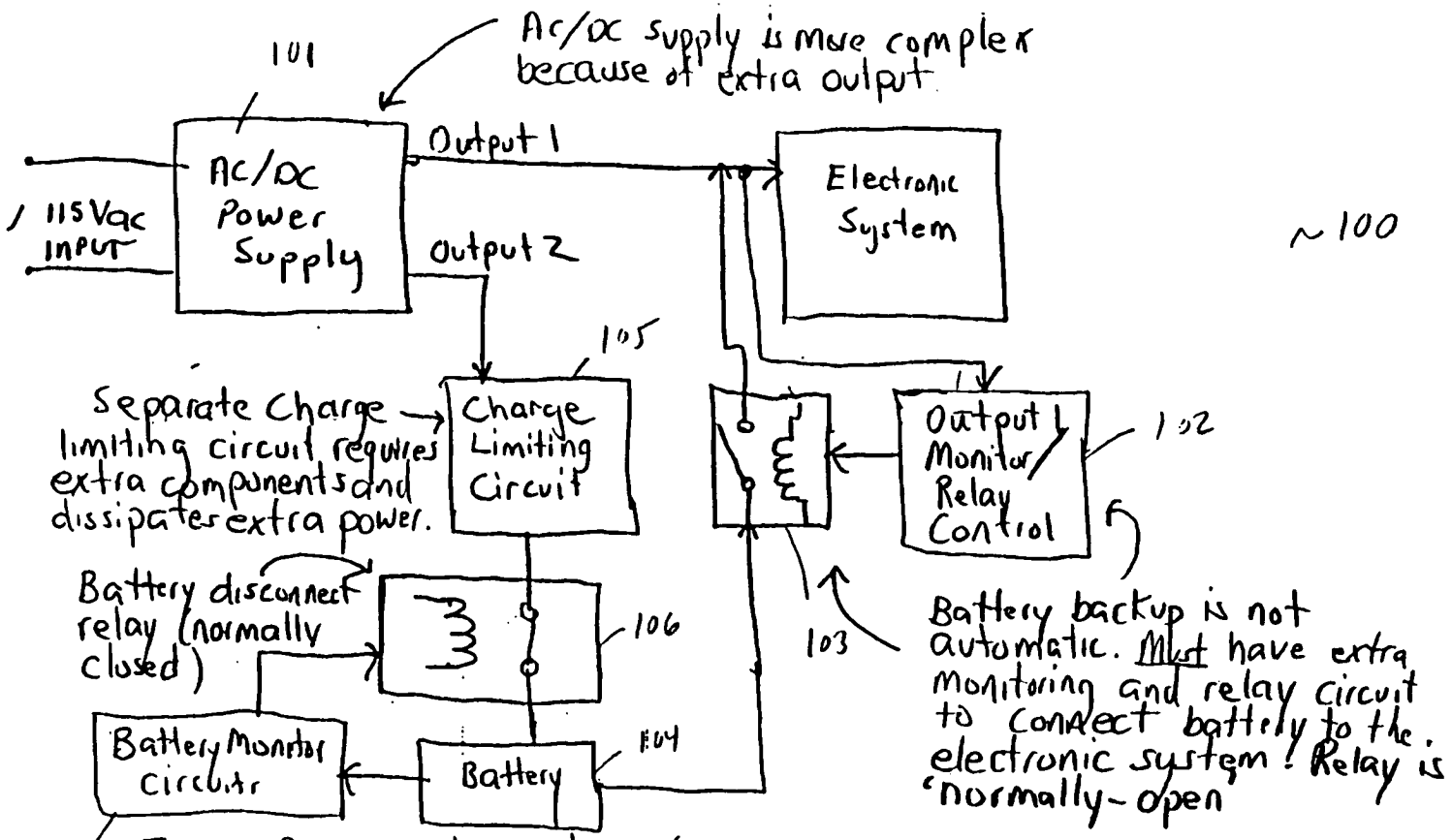


Figure 13 Conventional AC/DC Power Supply and Battery Backup System (PRIOR ART)

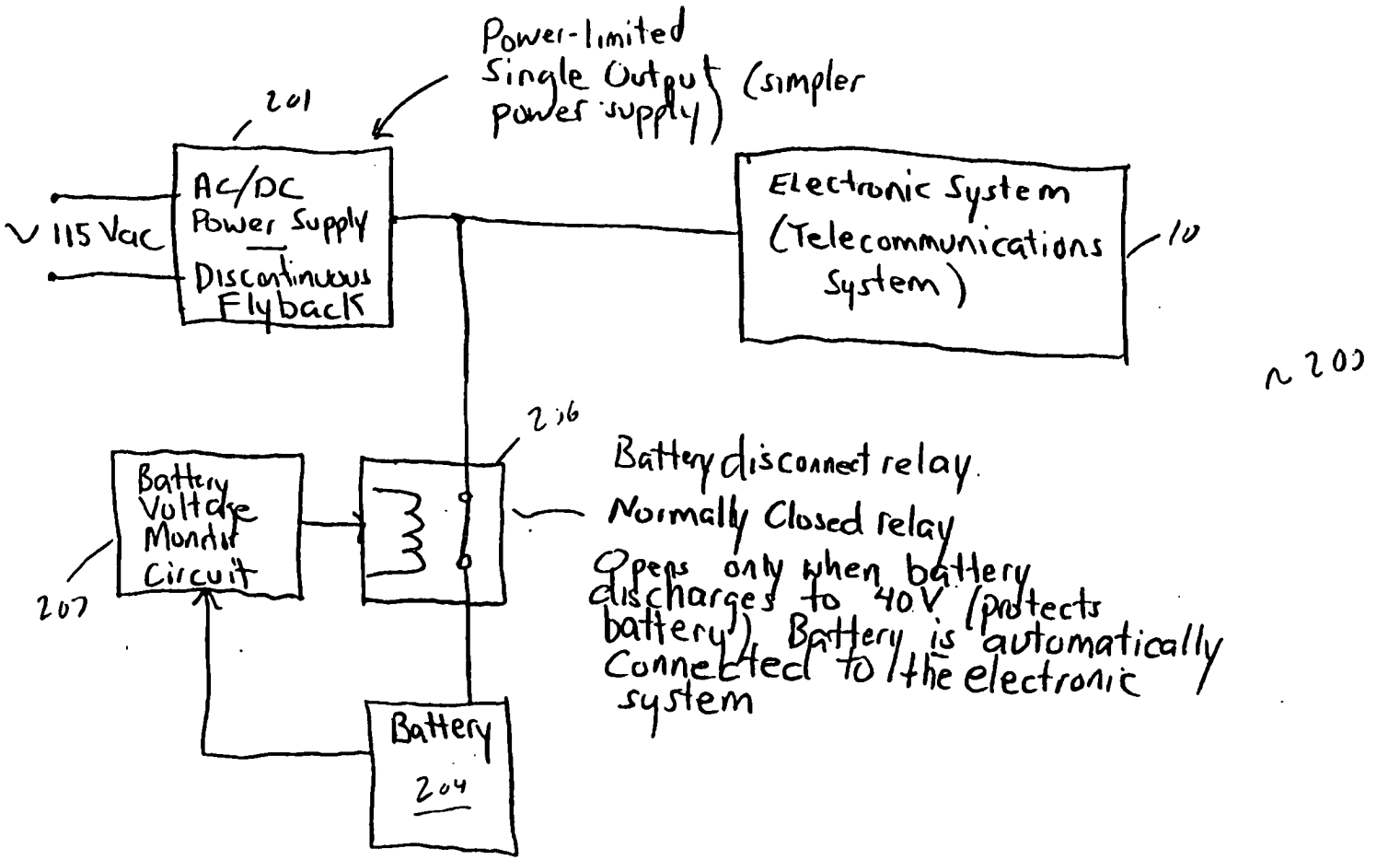


Figure 14 Block Diagram of New Power Supply/Battery Backup System

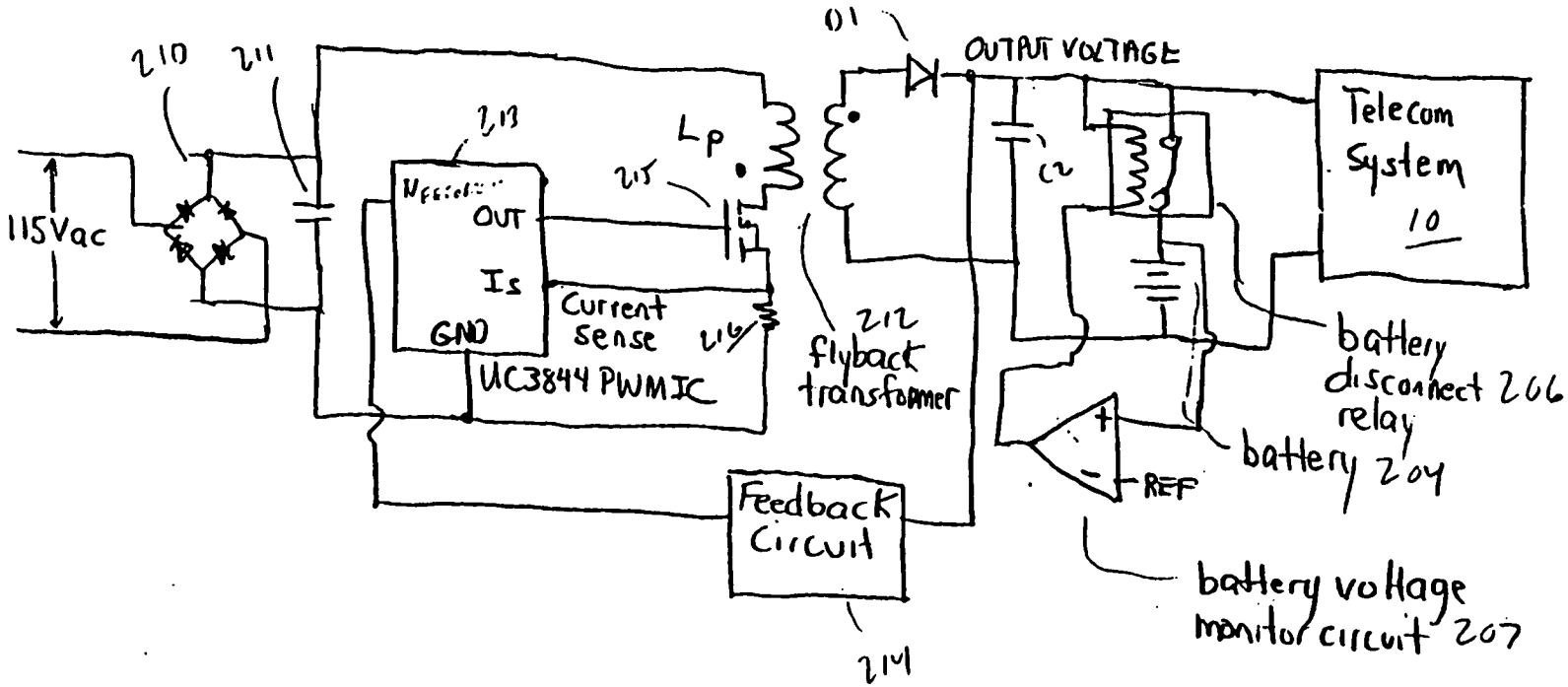


Figure 15 Simplified Schematic of New Power Supply/ Battery Backup System

~ 200

Timing Diagram for SPI Receive Status Interface with all Access Modules (8 Bits)
Data coming from Access Module

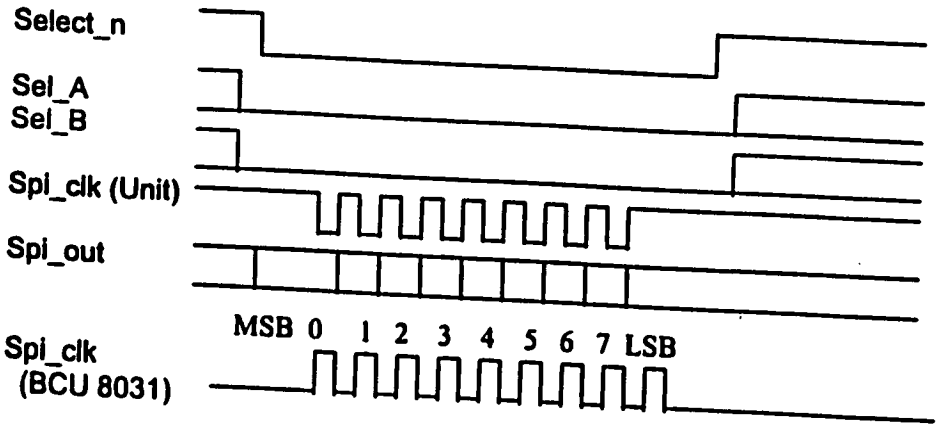


Figure 16

Timing Diagram for SPI Receive Interface from Smart Access Modules for Provisioning (9 Bits)
Data going into Access Module

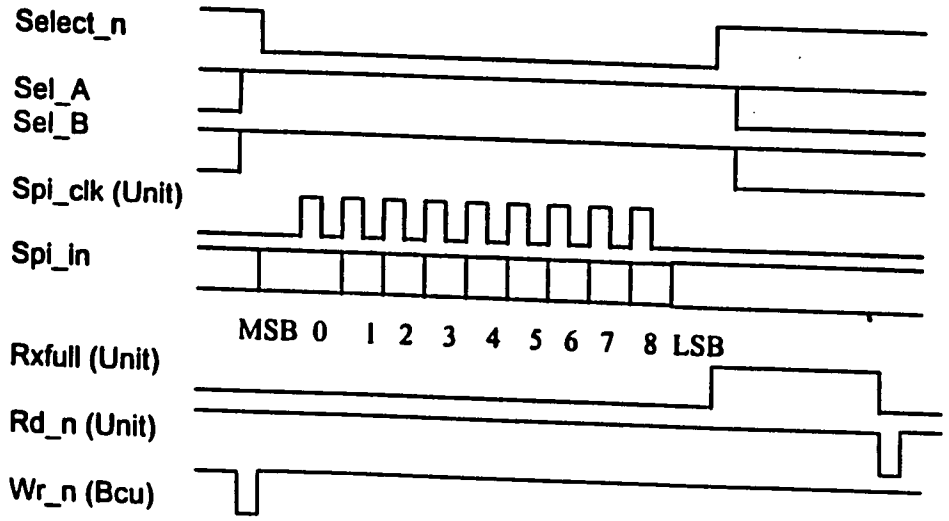


Figure 17

Timing Diagram for SPI Transmit Interface to Smart Access Modules for Provisioning (9 Bits)
Data coming from Access Module

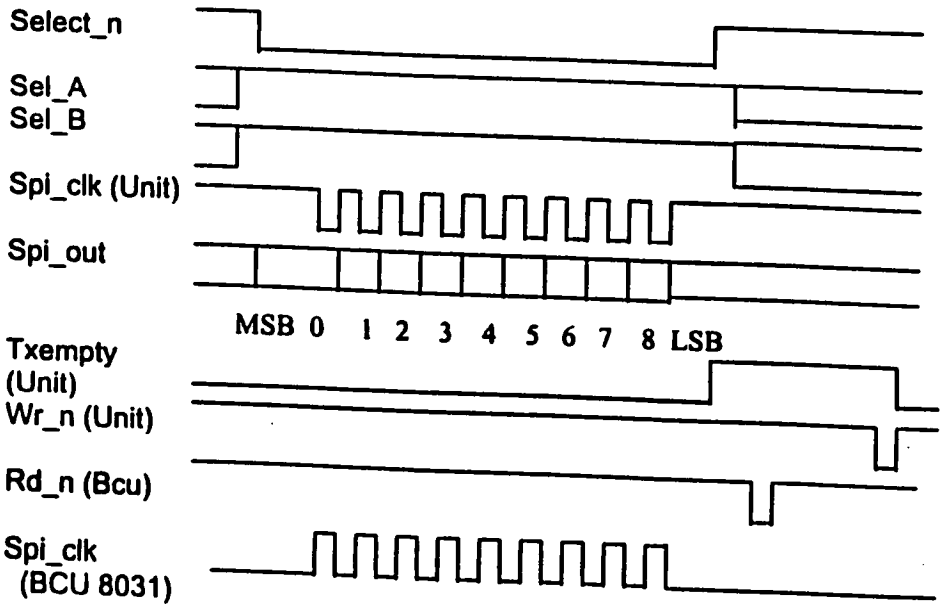


Figure 18

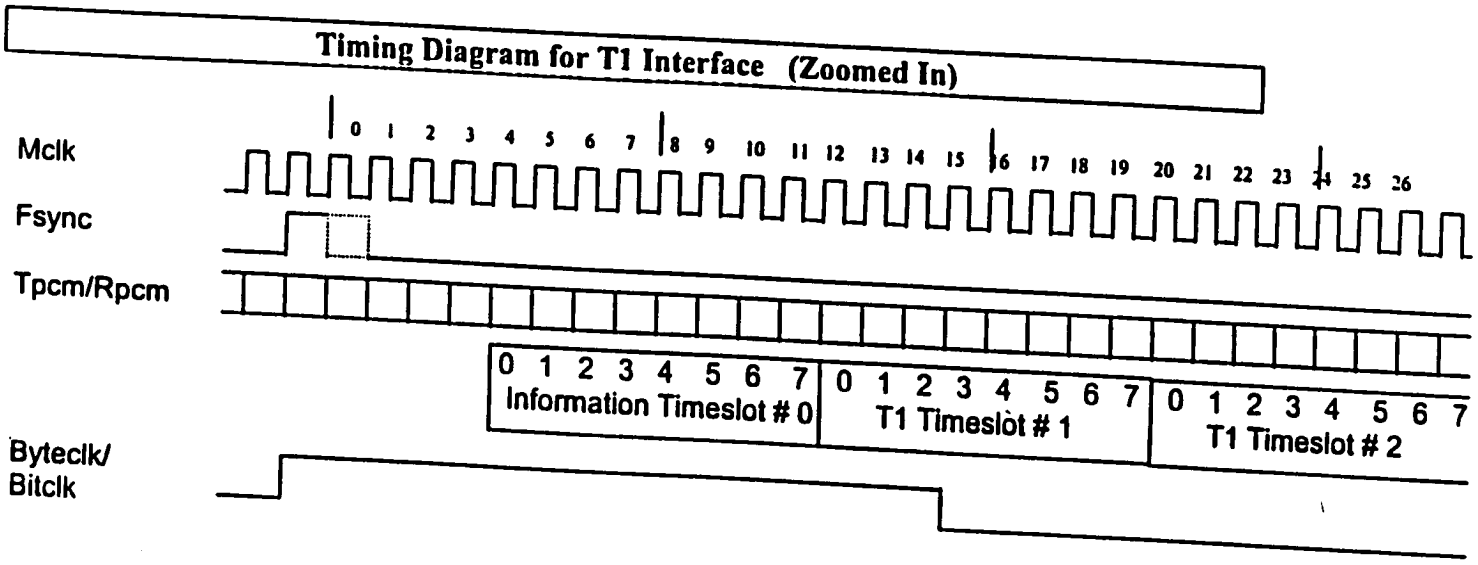

Timing Diagram for T1 Interface (Zoomed In)
Mclk
Fsync
Tpcm/Rpcm
Byteclk/
Bitclk
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
0 1 2 3 4 5 6 7
Information Timeslot # 0
0 1 2 3 4 5 6 7
T1 Timeslot # 1
0 1 2 3 4 5 6 7
T1 Timeslot # 2

Figure 19

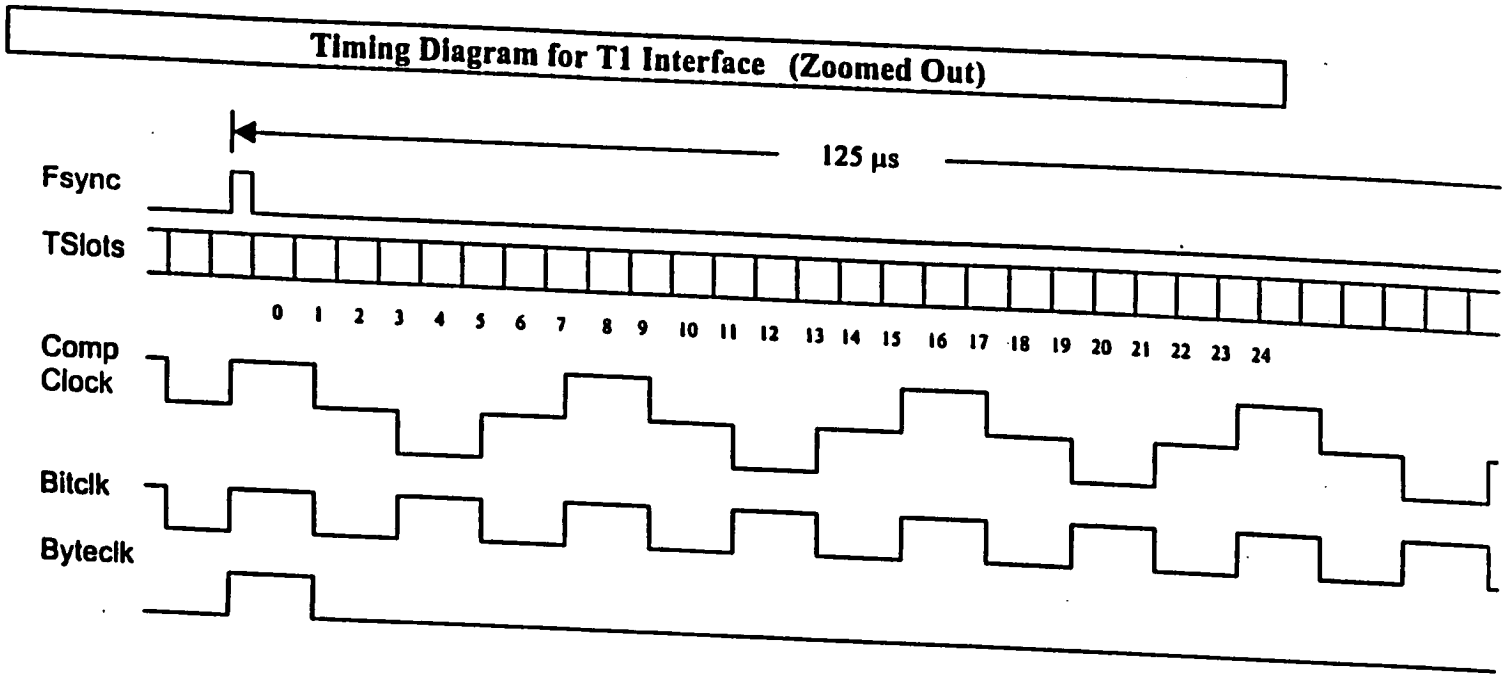

Timing Diagram for T1 Interface (Zoomed Out)
125 µs
Fsync
TSlots
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
Comp Clock
Bitclk
Byteclk

Figure 20